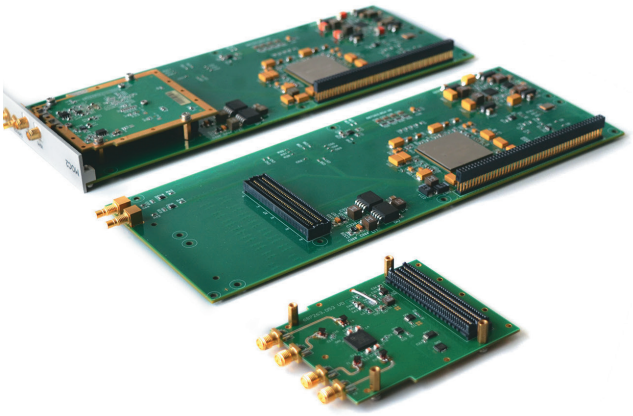
FPGA NM-FMC

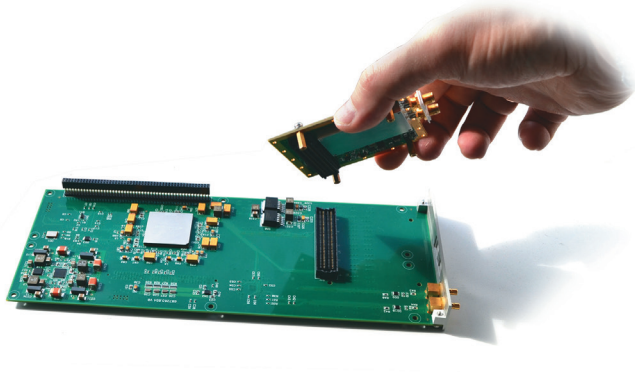
The NM-FMC mezzanine module is a convenient means by which users can independently implement their own algorithms for receiving, transmitting and digital information processing at the hardware level. The module contains an Altera FPGA of the Stratix III family, a clock generation unit, an 8 GB DDR3 memory and a 160-pin LPC connector for connecting FMC mezzanines.

Using the built-in VCO and integer dividers, the AD9516 clock circuit allows the generation of various clock frequencies from 10 MHz to 2.95 GHz, which, in combination with the PLL integrated in the FPGA, provides unlimited possibilities for generating the required clock grid. FPGA NM-FMC can operate both from the built-in 10 MHz reference generator with an accuracy of 1 × 10-6, and from external.

The built-in 60 Mbit FLASH memory is software accessible and is used both for storing FPGA firmware and for saving user data, for example, calibration coefficient tables.

Structurally, the module supports the installation of single FMC mezzanines (FPGA Mezzanine Card Standart ANSI / VITA 57.1) both





manufactured by Informtest and other manufacturers. To date, the Informtest holding has developed two types of FMC mezzanines:

- FMC AD9361 - a radio interface, a transceiver that receives and transmits radio signals in the frequency band from 70 MHz to 6 GHz with an instantaneous modulated signal band of up to 56 MHz.
- FMC AD6679 is a two-channel receiver-digitizer of a signal with a 14-bit ADC with a sampling frequency of 500 MHz for each channel and an analog signal band from 1 to 400 MHz.

If necessary, the user for his needs can independently develop a mezzanine according to the FMC specification or order its development from us.

FPGA NM-FMC can be installed on any of the existing Informtest holding mezzanine carriers made in VXI, LXI and AXIe standards. Including the latest NM AXI module, designed to work on the AXI express version 0 chassis and providing maximum performance when working with modular systems.

The package of FPGA NM-FMC includes all the necessary documentation, examples of FPGA projects and software in the VXI Plug & play standard, sufficient for the developer to focus on the development and implementation of his own algorithms, minimally taking care of the hardware and software components.

Specifications

<table>
<tr><td>FPGA module form factor
Double mezzanine</td><td>FPGA Type
Stratix III EP3SE50F780C2N</td></tr>
<tr><td rowspan="2">Number of FPGAs I / O Available to the FMC Connector
• 34 LVDS or 68 LVTTL2.5 or LVTTL3.3;
• 2 frequency inputs from the mezzanine FMC LVDS / LVPECL</td><td>RPZU volume
64 Mbps memory type FLASH</td></tr>
<tr><td>RAM amount
8 GB DDR3 memory type</td></tr>
<tr><td>RAM data bus width
64 bit</td><td>The maximum frequency of RAM
700 MHz DDR</td></tr>
<tr><td rowspan="2">VCO Frequency Range:
• AD9516-0 - 2550 – 2950 MHz
• AD9516-1 - 2300 – 2650 MHz
• AD9516-2 - 2050 – 2330 MHz
• AD9516-3 - 2550 – 2950 MHz
• AD9516-4 - 1450 – 1800 MHz
At the choice of the user, any of these generators can be installed</td><td>Maximum bandwidth of the FPGA-RAM channel (with packet writing or reading)
40 Gbps</td></tr>
<tr><td>Maximum FIFO bus bandwidth (between FPGA and user program when working on Ethernet 100 Base-T / 1000 Base-T
• 40 MB / s on MezaBOX-4M LXI
• 4 MB / s on MezaBOX-LXI</td></tr>
<tr><td>VCO Division Factors 1 - 5</td><td>The division ratios of the outputs of the generator
1 to 32</td></tr>
<tr><td colspan="2">Supply voltage FMC mezzanine
• +12 B @ 2 A
• +3,3 B @ 1 A
• +2,5 B (VADJ) @ 1 A</td></tr>
</table>