Transceiver **MT**

Mezzanine MT (mezzanine transceiver) is designed to receive and transmit microwave signals in the frequency range from 70 to 6000 MHz. The MT transceiver is a new generation device developed using the most advanced element base and designed for use in modern measuring systems built on the basis of open standards AXIe, VXI and LXI.

Based on this module, transceivers with various types of quadrature modulations, both standard and customer specifications, can be implemented.

Also, one of the many applications of this transceiver is to create a complex for checking the quality of radio path channels.

PRINCIPLE OF OPERATION:

From the FPGA output to the AD9361 transceiver chip, a modulated quadrature signal is received in digital representation via digital channel P0. The transceiver transfers the signal to the programmed carrier frequency of the transmitter. At the same time, the receiving channel AD9361 transfers the signal received at the carrier frequency to the low-frequency range and digitally transmits the quadrature signal via digital channel P1 to the FPGA, where it is demodulated. Both channels of the transceiver operate in the FDD frequency separation mode so that different values of the carrier frequencies can be set for the receiver and transmitter. The MT driver contains the complete API of the AD9361 chip for finer tuning of the transmit / receive process.

- 56 MHz Radio Band
- Frequency range from 70 to 6000 MHz
- Quadrature signal, DAC / ADC resolution 12 bits
- Sampling Rate 61.44 MS/s
- RAM 4 GSamples

The basis of the digital part of the mezzanine is a high-speed FPGA that implements:

- Receiving data packets through the mezzanine carrier interface (MezaBOX-4M LXI) for the transmitter and storing them in the mezzanine RAM for subsequent delivery via the microwave channel;
- Continuous delivery of data received via the microwave channel via the mezzanine carrier interface;
- Digital modulation / demodulation of data;
- Management of transceiver operating modes and analog nodes;
- Synchronization of transmission / reception channels of several mezzanines;
- FPGA implementation of custom data processing algorithms.

Specifications

Implementation based on the AD9361 chip manufactured by Analog Devices	Contains one transmitter channel and one receiver channel
Operating frequency range from 70 MHz to 6 GHz	Frequency setting step no more than 50 Hz
Frequency setting accuracy, during operation: • from the internal 10 MHz generator is not worse ± 2×10^{-6}; • from an external generator (10 MHz, 100 MHz) is not worse ± 3×10^{-8}	The maximum instantaneous bandwidth of the output and received modulated signal is not less than 56 MHz
The maximum output level of the transmitter is at least 5 dBm	Transmitter signal level adjustment range 90 dB in 0.25 dB increments
RAM for storing information for transmission and reception with a total volume of 8 Gb	Receiving information on the microwave path at the input signal level from -60 to 0 dBm
Continuous reception mode without loss of information at a speed of information flow of no more than 40 Mbit / s	AM, PM and FM modulation / demodulation of the digital stream. The ability to add different types of quadrature modulation at the request of the customer